Compact, 600 mA, 3 MHz, Step-Down DC-to-DC Converter

Data Sheet

ADP2108

FEATURES

Peak efficiency: 95%
3 MHz fixed frequency operation
Typical quiescent current: 18 µA
Maximum load current: 600 mA
Input voltage: 2.3 V to 5.5 V
Uses tiny multilayer inductors and capacitors
Current mode architecture for fast load and line transient response
100% duty cycle low dropout mode
Internal synchronous rectifier
Internal compensation
Internal soft start
Current overload protection
Thermal shutdown protection
Shutdown supply current: 0.2 µA
Available in
- **5-ball WLCSP**
- **5-lead TSOT**

Supported by ADIsimPower™ design tool

APPLICATIONS

PDAs and palmtop computers
Wireless handsets
Digital audio, portable media players
Digital cameras, GPS navigation units

GENERAL DESCRIPTION

The ADP2108 is a high efficiency, low quiescent current step-down dc-to-dc converter manufactured in two different packages. The total solution requires only three tiny external components. It uses a proprietary, high speed current mode, constant frequency PWM control scheme for excellent stability and transient response. To ensure the longest battery life in portable applications, the ADP2108 has a power save mode that reduces the switching frequency under light load conditions.

The ADP2108 runs on input voltages of 2.3 V to 5.5 V, which allows for single lithium or lithium polymer cell, multiple alkaline or NiMH cell, PCMCIA, USB, and other standard power sources. The maximum load current of 600 mA is achievable across the input voltage range.

The ADP2108 is available in fixed output voltages of 3.3 V, 3.0 V, 2.5 V, 2.3 V, 1.82 V, 1.8 V, 1.5 V, 1.3 V, 1.2 V, 1.1 V, and 1.0 V. All versions include an internal power switch and synchronous rectifier for minimal external part count and high efficiency. The ADP2108 has an internal soft start and is internally compensated. During logic controlled shutdown, the input is disconnected from the output and the ADP2108 draws less than 1 µA from the input source.

Other key features include undervoltage lockout to prevent deep battery discharge and soft start to prevent input current overshoot at startup. The ADP2108 is available in 5-ball WLCSP and 5-lead TSOT packages. The ADP2109 provides the same features and operations as the ADP2108 and has the additional function of a discharge switch in the WLCSP package.

TYPICAL APPLICATIONS CIRCUIT

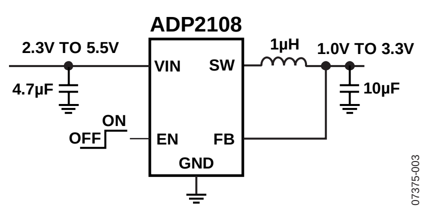


Figure 1.

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Technical Support
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1/12—Rev. E to Rev. F

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10/10—Rev. D to Rev. E

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9/08—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 3.6 V, V_{OUT} = 1.8 V, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.[1]

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Input Voltage Range		2.3		5.5	V
Undervoltage Lockout Threshold	V_{IN} rising			2.3	V
	V_{IN} falling	2.05	2.15	2.25	V
OUTPUT CHARACTERISTICS					
Output Voltage Accuracy	PWM mode	−2		+2	%
	V_{IN} = 2.3 V to 5.5 V, PWM mode	−2.5		+2.5	%
POWER SAVE MODE TO PWM CURRENT THRESHOLD			85		mA
PWM TO POWER SAVE MODE CURRENT THRESHOLD			80		mA
INPUT CURRENT CHARACTERISTICS					
DC Operating Current	I_{LOAD} = 0 mA, device not switching		18	30	µA
Shutdown Current	EN = 0 V, T_A = T_J = −40°C to +125°C		0.2	1.0	µA
SW CHARACTERISTICS					
SW On Resistance (WLCSP)	PFET		320		mΩ
	NFET		300		mΩ
SW On Resistance (TSOT)	PFET		380		mΩ
	NFET		260		mΩ
Current Limit	PFET switch peak current limit	1100	1300	1500	mA
ENABLE CHARACTERISTICS					
EN Input High Threshold		1.2			V
EN Input Low Threshold				0.4	V
EN Input Leakage Current	EN = 0 V, 3.6 V	−1	0	+1	µA
OSCILLATOR FREQUENCY	I_{LOAD} = 200 mA	2.5	3.0	3.5	MHz
START-UP TIME				550	µs
THERMAL CHARACTERISTICS					
Thermal Shutdown Threshold			150		°C
Thermal Shutdown Hysteresis			20		°C

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN, EN	−0.4 V to +6.5 V
FB, SW to GND	−1.0 V to (V_{IN} + 0.2 V)
Operating Ambient Temperature Range	−40°C to +125°C
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range	−65°C to +150°C
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD Human Body Model	±1500 V
ESD Charged Device Model	±500 V
ESD Machine Model	±100 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all other voltages are referenced to GND.

The ADP2108 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated.

In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation (P_D) of the device, and the junction-to-ambient thermal resistance of the package (θ_{JA}). Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the formula

$$T_J = T_A + (P_D \times \theta_{JA}).$$

THERMAL RESISTANCE

θ_{JA} is specified for a device mounted on a JEDEC 2S2P PCB.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
5-Ball WLCSP	105	°C/W
5-Lead TSOT	170	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

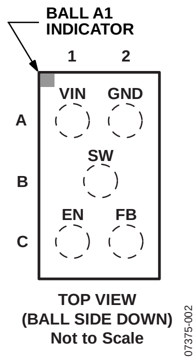


Figure 2. WLCSP Pin Configuration

Table 4. WLCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	VIN	Power Source Input. VIN is the source of the PFET high-side switch. Bypass VIN to GND with a 2.2 µF or greater capacitor as close to the ADP2108 as possible.
A2	GND	Ground. Connect all the input and output capacitors to GND.
B	SW	Switch Node Output. SW is the drain of the PFET switch and NFET synchronous rectifier.
C1	EN	Enable Input. Drive EN high to turn on the ADP2108. Drive EN low to turn it off and reduce the input current to 0.2 µA.
C2	FB	Feedback Input of the Error Amplifier. Connect FB to the output of the switching regulator.

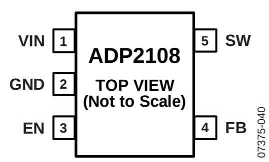


Figure 3. TSOT Pin Configuration

Table 5. TSOT Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VIN	Power Source Input. VIN is the source of the PFET high-side switch. Bypass VIN to GND with a 2.2 µf or greater capacitor as close to the ADP2108 as possible.
2	GND	Ground. Connect all the input and output capacitors to GND.
3	EN	Enable Input. Drive EN high to turn on the ADP2108. Drive EN low to turn it off and reduce the input current to 0.1 µA.
4	FB	Feedback Input of the Error Amplifier. Connect FB to the output of the switching regulator.
5	SW	Switch Node Output. SW is the drain of the PFET switch and NFET synchronous rectifier.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.6 V, T_A = 25°C, V_{EN} = V_{IN}, unless otherwise noted.

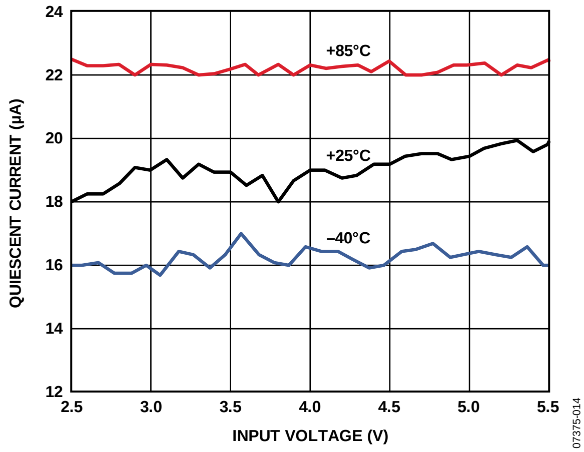


Figure 4. Quiescent Supply Current vs. Input Voltage

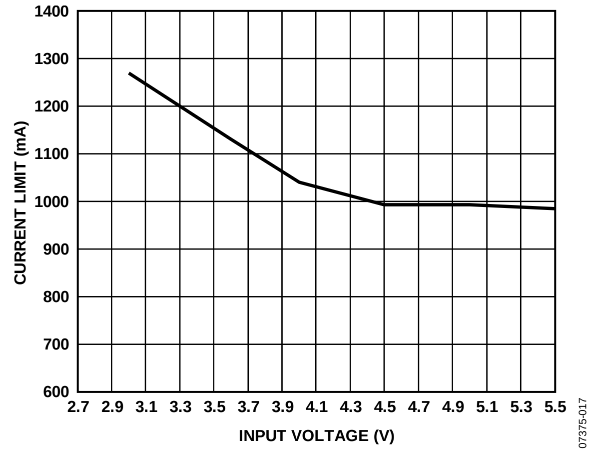


Figure 7. PMOS Current Limit vs. Input Voltage

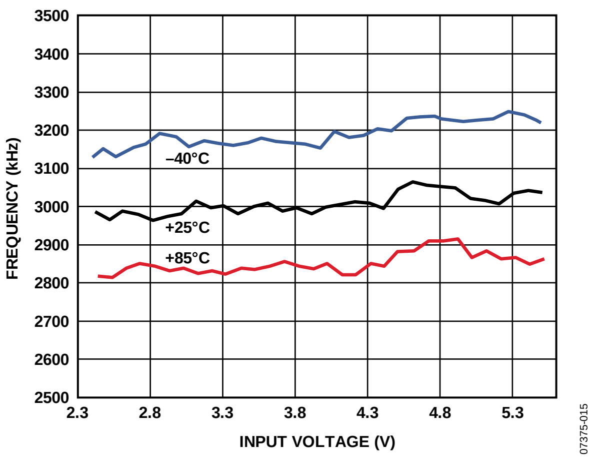


Figure 5. Switching Frequency vs. Input Voltage

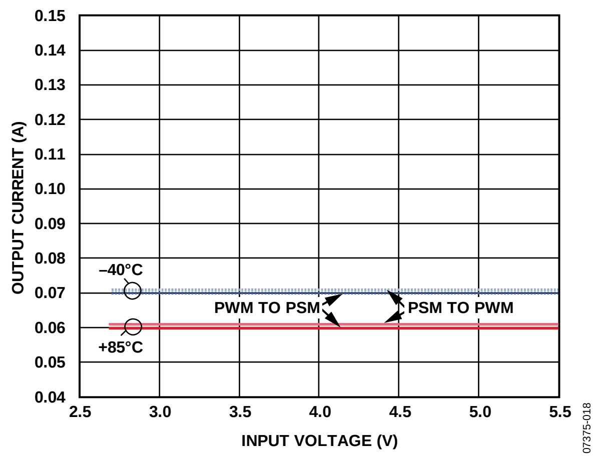


Figure 8. Mode Transition Across Temperature

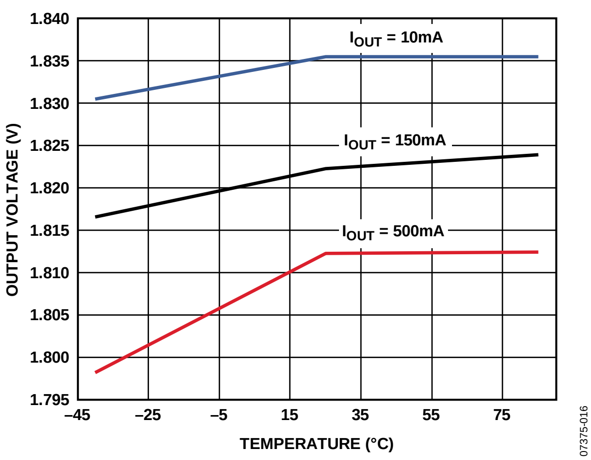


Figure 6. Output Voltage vs. Temperature

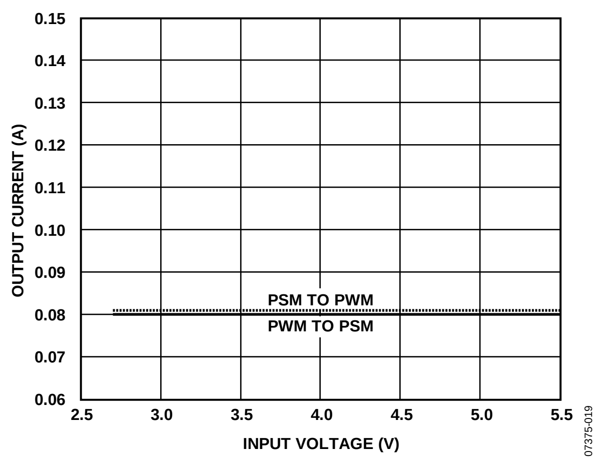


Figure 9. Mode Transition

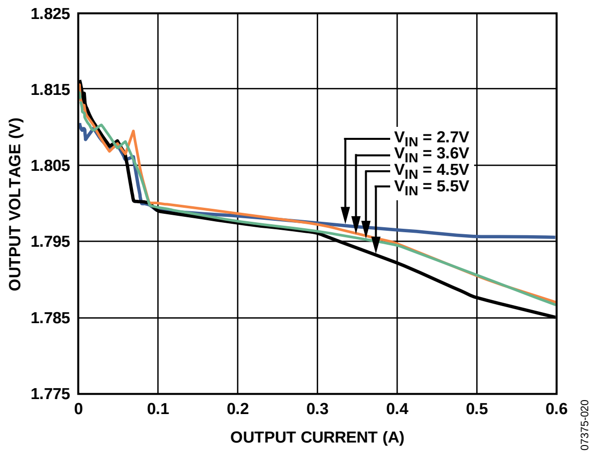


Figure 10. Load Regulation, V_{OUT} = 1.8 V

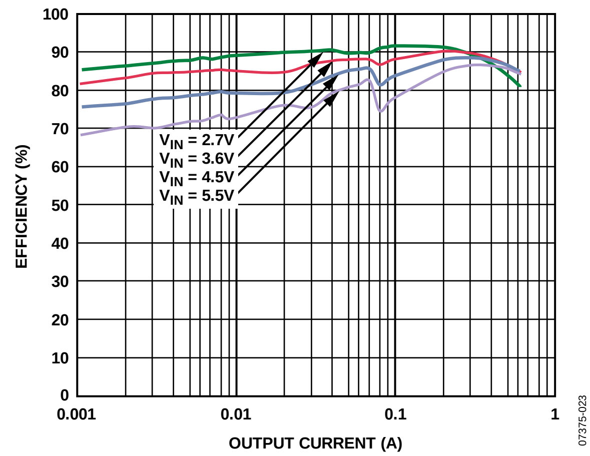


Figure 13. Efficiency, V_{OUT} = 1.8 V

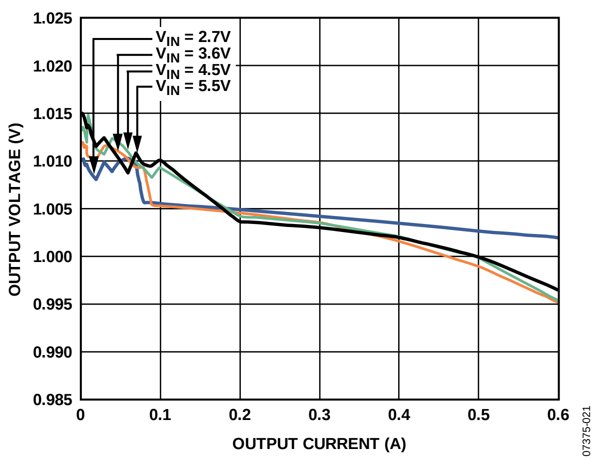


Figure 11. Load Regulation, V_{OUT} = 1.0 V

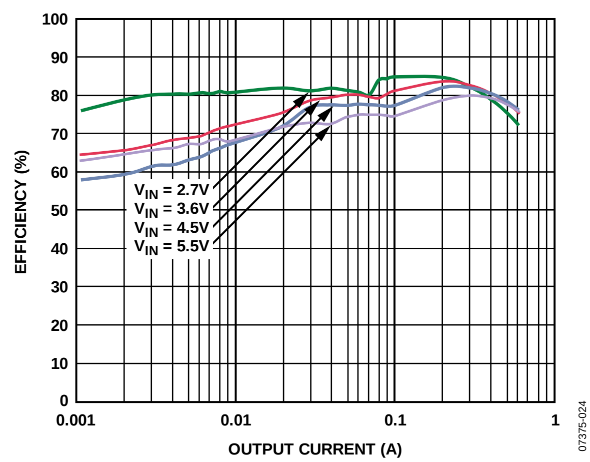


Figure 14. Efficiency, V_{OUT} = 1.0 V

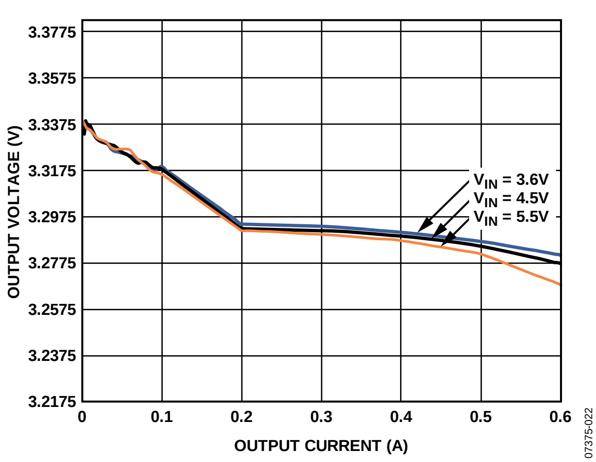


Figure 12. Load Regulation, V_{OUT} = 3.3 V

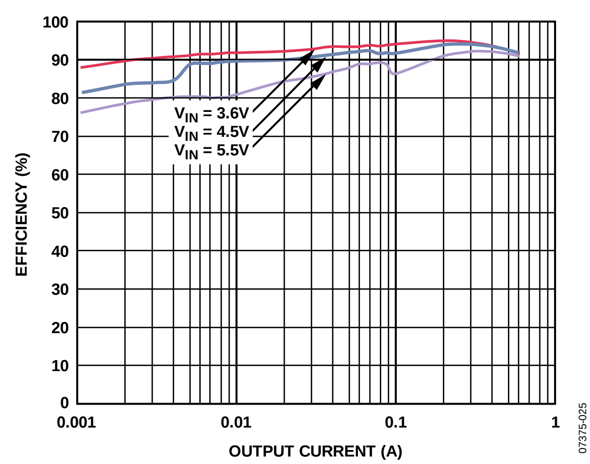


Figure 15. Efficiency, V_{OUT} = 3.3 V

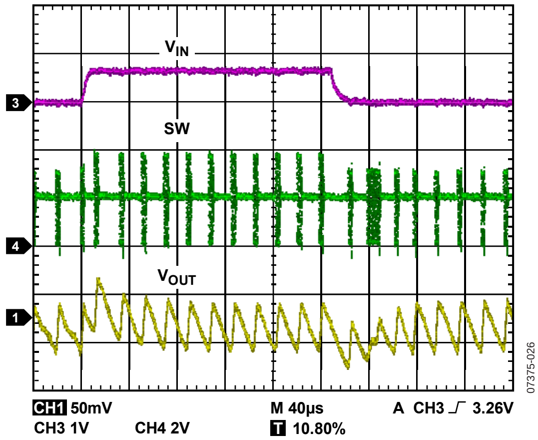


Figure 16. Line Transient, V_{OUT} = 1.8 V, Power Save Mode, 20 mA

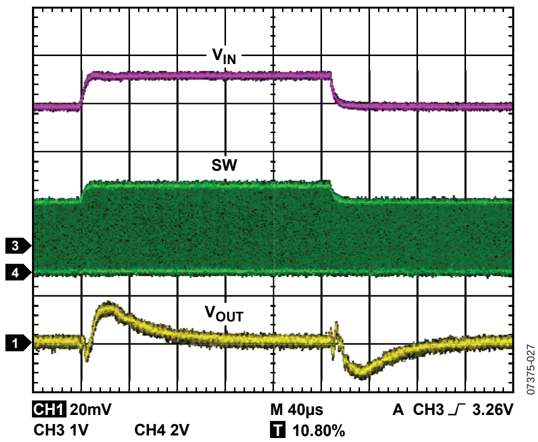


Figure 17. Line Transient, V_{OUT} = 1.8 V, PWM, 200 mA

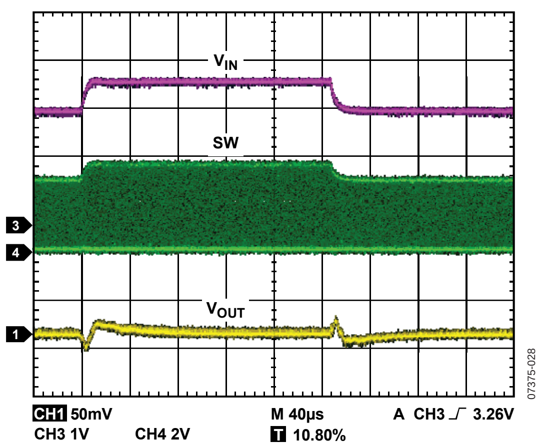


Figure 18. Line Transient, V_{OUT} = 1.0 V, PWM, 200 mA

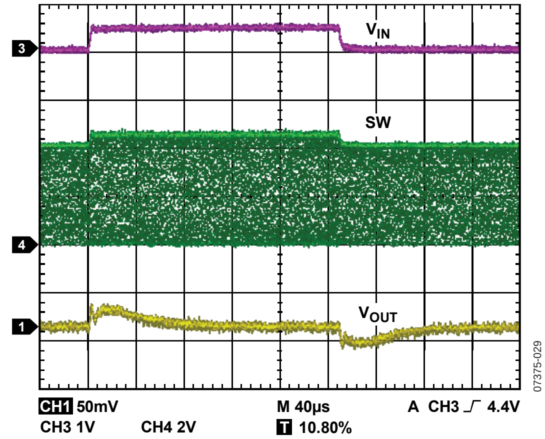


Figure 19. Line Transient, V_{OUT} = 3.3 V, PWM, 200 mA

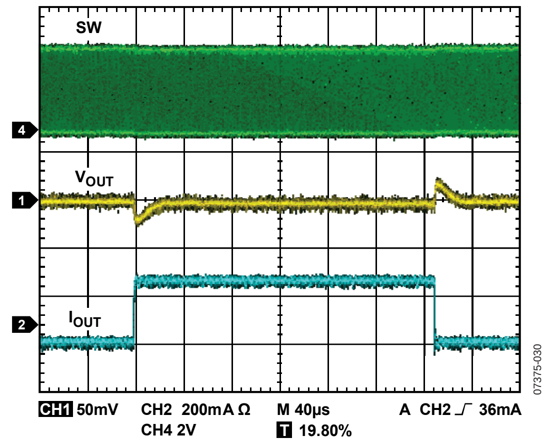


Figure 20. Load Transient, V_{OUT} = 1.8 V, 300 mA to 600 mA

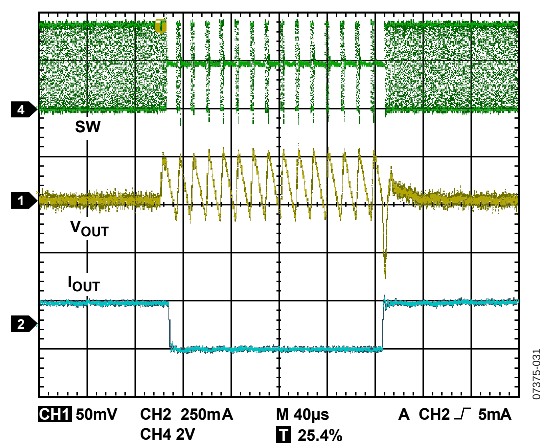


Figure 21. Load Transient, V_{OUT} = 1.8 V, 50 mA to 300 mA

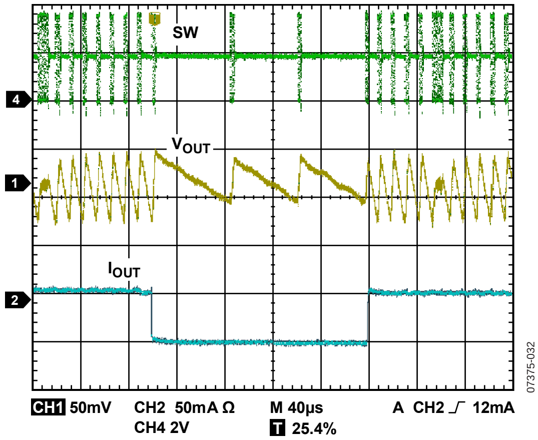


Figure 22. Load Transient, V_{OUT} = 1.8 V, 5 mA to 50 mA

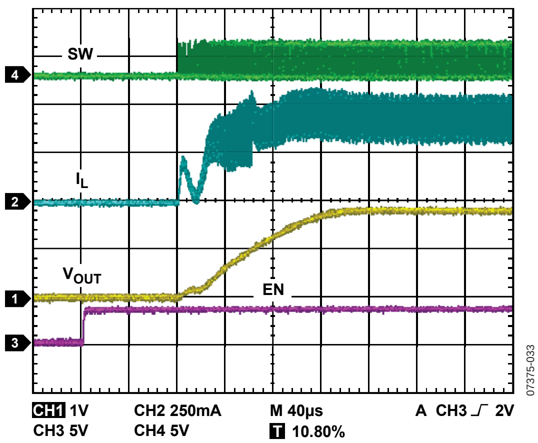


Figure 23. Start-Up, V_{OUT} = 1.8 V, 400 mA

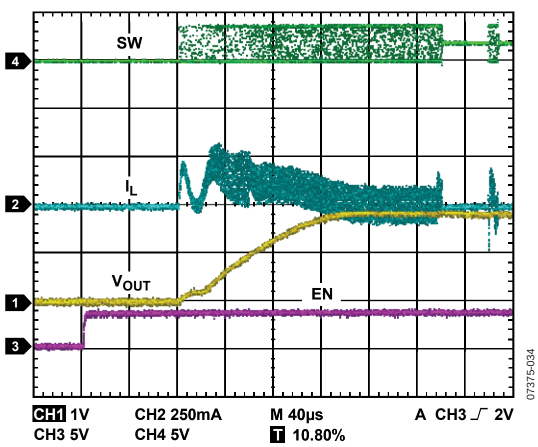


Figure 24. Start-Up, V_{OUT} = 1.8 V, 5 mA

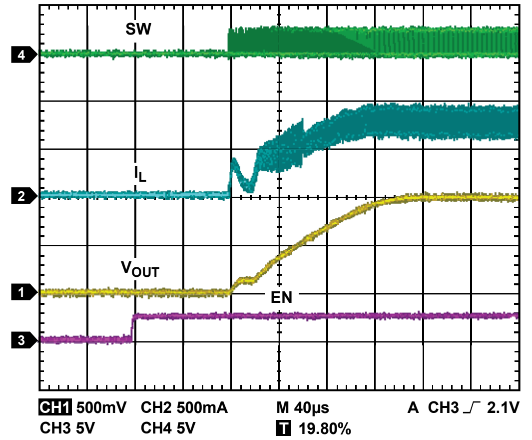


Figure 25. Start-Up, V_{OUT} = 1.0 V, 600 mA

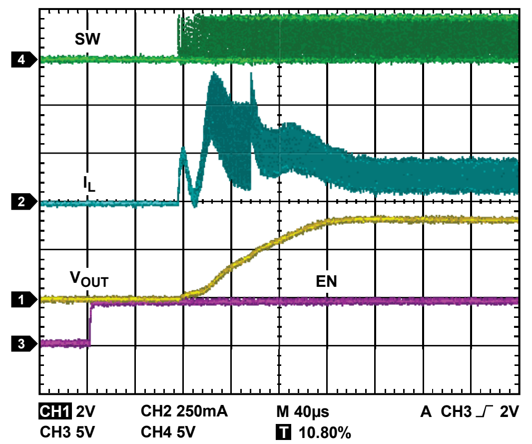


Figure 26. Start-Up, V_{OUT} = 3.3 V, 150 mA

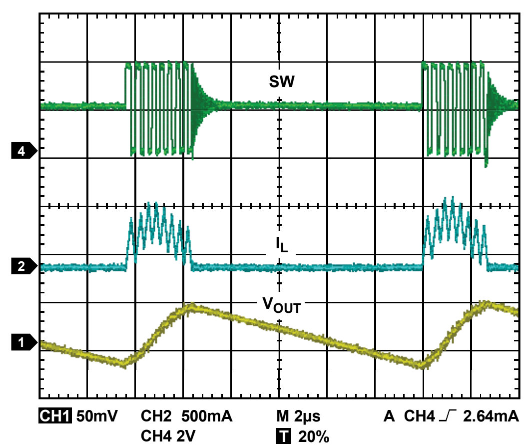


Figure 27. Typical Power Save Mode Waveform, 50 mA

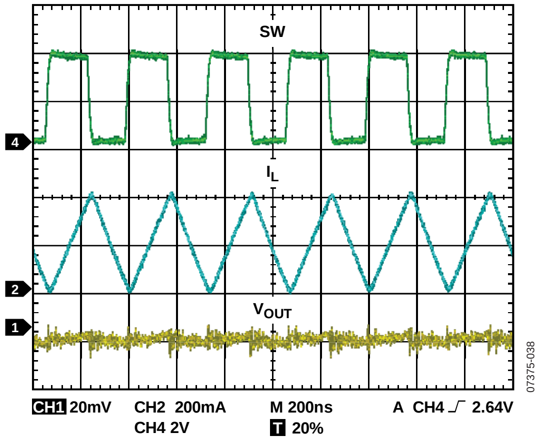


Figure 28. Typical PWM Waveform, 200 mA

THEORY OF OPERATION

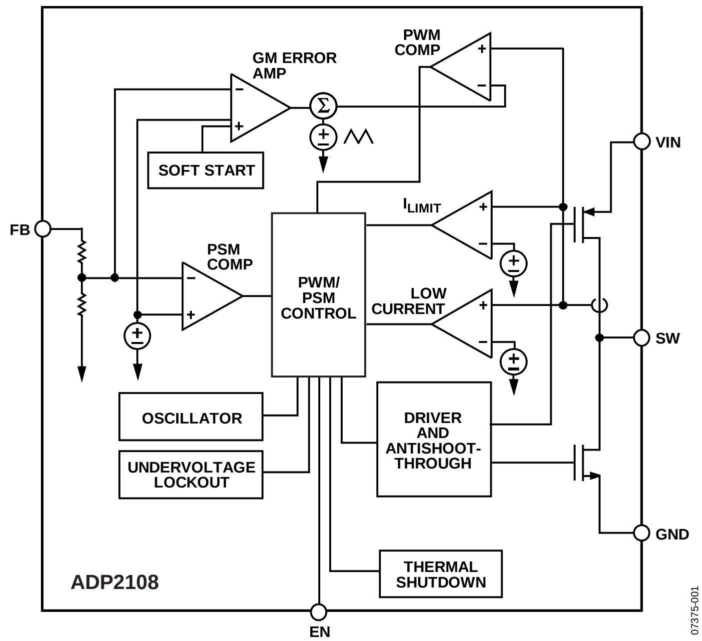


Figure 29. Functional Block Diagram

The ADP2108 is a step-down dc-to-dc converter that uses a fixed frequency and high speed current mode architecture. The high switching frequency allows for a small step-down, dc-to-dc converter solution.

The ADP2108 operates with an input voltage of 2.3 V to 5.5 V and regulates an output voltage down to 1.0 V.

CONTROL SCHEME

The ADP2108 operates with a fixed frequency, current mode PWM control architecture at medium to high loads for high efficiency, but shifts to a power save mode control scheme at light loads to lower the regulation power losses. When operating in fixed frequency PWM mode, the duty cycle of the integrated switches is adjusted and regulates the output voltage. When operating in power save mode at light loads, the output voltage is controlled in a hysteretic manner, with higher V_{OUT} ripple. During part of this time, the converter is able to stop switching and enters an idle mode, which improves conversion efficiency.

PWM MODE

In PWM mode, the ADP2108 operates at a fixed frequency of 3 MHz, set by an internal oscillator. At the start of each oscillator cycle, the PFET switch is turned on, sending a positive voltage across the inductor. Current in the inductor increases until the current sense signal crosses the peak inductor current threshold that turns off the PFET switch and turns on the NFET synchronous rectifier. This sends a negative voltage across the inductor, causing the inductor current to decrease. The synchronous rectifier stays on for the rest of the cycle. The ADP2108 regulates the output voltage by adjusting the peak inductor current threshold.

POWER SAVE MODE

The ADP2108 smoothly transitions to the power save mode of operation when the load current decreases below the power save mode current threshold. When the ADP2108 enters power save mode, an offset is induced in the PWM regulation level, which makes the output voltage rise. When the output voltage reaches a level approximately 1.5% above the PWM regulation level, PWM operation is turned off. At this point, both power switches are off, and the ADP2108 enters an idle mode. C_{OUT} discharges until V_{OUT} falls to the PWM regulation voltage, at which point the device drives the inductor to make V_{OUT} rise again to the upper threshold. This process is repeated while the load current is below the power save mode current threshold.

Power Save Mode Current Threshold

The power save mode current threshold is set to 80 mA. The ADP2108 employs a scheme that enables this current to remain accurately controlled, independent of V_{IN} and V_{OUT} levels. This scheme also ensures that there is very little hysteresis between the power save mode current threshold for entry to and exit from the power save mode. The power save mode current threshold is optimized for excellent efficiency over all load currents.

ENABLE/SHUTDOWN

The ADP2108 starts operation with soft start when the EN pin is toggled from logic low to logic high. Pulling the EN pin low forces the device into shutdown mode, reducing the shutdown current below 1 μA.

SHORT-CIRCUIT PROTECTION

The ADP2108 includes frequency foldback to prevent output current runaway on a hard short. When the voltage at the feedback pin falls below half the target output voltage, indicating the possibility of a hard short at the output, the switching frequency is reduced to half the internal oscillator frequency. The reduction in the switching frequency allows more time for the inductor to discharge, preventing a runaway of output current.

UNDERVOLTAGE LOCKOUT

To protect against battery discharge, undervoltage lockout (UVLO) circuitry is integrated on the ADP2108. If the input voltage drops below the 2.15 V UVLO threshold, the ADP2108 shuts down, and both the power switch and the synchronous rectifier turn off. When the voltage rises above the UVLO threshold, the soft start period is initiated, and the part is enabled.

THERMAL PROTECTION

In the event that the ADP2108 junction temperature rises above 150°C, the thermal shutdown circuit turns off the converter. Extreme junction temperatures can be the result of high current operation, poor circuit board design, or high ambient temperature. A 20°C hysteresis is included so that when thermal shutdown occurs, the ADP2108 does not return to operation until the on-chip temperature drops below 130°C. When coming out of thermal shutdown, soft start is initiated.

SOFT START

The ADP2108 has an internal soft start function that ramps the output voltage in a controlled manner upon startup, thereby limiting the inrush current. This prevents possible input voltage drops when a battery or a high impedance power source is connected to the input of the converter.

After the EN pin is driven high, internal circuits start to power up. The time required to settle after the EN pin is driven high is called the power-up time. After the internal circuits are powered up, the soft start ramp is initiated and the output capacitor is charged linearly until the output voltage is in regulation. The time required for the output voltage to ramp is called the soft start time.

Start-up time in the ADP2108 is the measure of when the output is in regulation after the EN pin is driven high. Start-up time consists of the power-up time and the soft start time.

CURRENT LIMIT

The ADP2108 has protection circuitry to limit the amount of positive current flowing through the PFET switch and the synchronous rectifier. The positive current limit on the power switch limits the amount of current that can flow from the input to the output. The negative current limit prevents the inductor current from reversing direction and flowing out of the load.

100% DUTY OPERATION

With a drop in V_{IN} or with an increase in I_{LOAD}, the ADP2108 reaches a limit where, even with the PFET switch on 100% of the time, V_{OUT} drops below the desired output voltage. At this limit, the ADP2108 smoothly transitions to a mode where the PFET switch stays on 100% of the time. When the input conditions change again and the required duty cycle falls, the ADP2108 immediately restarts PWM regulation without allowing overshoot on V_{OUT}.

APPLICATIONS INFORMATION

ADIsimPower DESIGN TOOL

The ADP2108 is supported by ADIsimPower design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic, bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count while taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about ADIsimPower design tools, refer to www.analog.com/ADIsimPower. The tool set is available from this website, and users can also request an unpopulated board through the tool.

EXTERNAL COMPONENT SELECTION

Trade-offs between performance parameters such as efficiency and transient response can be made by varying the choice of external components in the applications circuit, as shown in Figure 1.

Inductor

The high switching frequency of the ADP2108 allows for the selection of small chip inductors. For best performance, use inductor values between 0.7 µH and 3 µH. Recommended inductors are shown in Table 6.

The peak-to-peak inductor current ripple is calculated using the following equation:

$$I_{RIPPLE} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

where:
f_{SW} is the switching frequency.
L is the inductor value.

The minimum dc current rating of the inductor must be greater than the inductor peak current. The inductor peak current is calculated using the following equation:

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{I_{RIPPLE}}{2}$$

Inductor conduction losses are caused by the flow of current through the inductor, which has an associated internal DCR. Larger sized inductors have smaller DCR, which may decrease inductor conduction losses. Inductor core losses are related to the magnetic permeability of the core material. Because the ADP2108 is a high switching frequency dc-to-dc converter, shielded ferrite core material is recommended for its low core losses and low EMI.

Table 6. Suggested 1.0 µH Inductors

Vendor	Model	Dimensions	I_{SAT} (mA)	DCR (mΩ)
Murata	LQM21PN1R0M	2.0 × 1.25 × 0.5	800	190
Murata	LQM31PN1R0M	3.2 × 1.6 × 0.85	1200	120
Murata	LQM2HPN1R0M	2.5 × 2.0 × 1.1	1500	90
Coilcraft	LPS3010-102	3.0 × 3.0 × 0.9	1700	85
Toko	MDT2520-CN	2.5 × 2.0 × 1.2	1800	100
TDK	CPL2512T	2.5 × 1.5 × 1.2	1500	100

Output Capacitor

Higher output capacitor values reduce the output voltage ripple and improve load transient response. When choosing this value, it is also important to account for the loss of capacitance due to output voltage dc bias.

Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended for best performance. Y5V and Z5U dielectrics are not recommended for use with any dc-to-dc converter because of their poor temperature and dc bias characteristics.

The worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage is calculated using the following equation:

$$C_{EFF} = C_{OUT} \times (1 - TEMPCO) \times (1 - TOL)$$

where:
C_{EFF} is the effective capacitance at the operating voltage.
$TEMPCO$ is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +125°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{OUT} is 9.2 µF at 1.8 V, as shown in Figure 30.

Substituting these values in the equation yields

$$C_{EFF} = 9.2\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 7.0\ \mu F$$

To guarantee the performance of the ADP2108, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

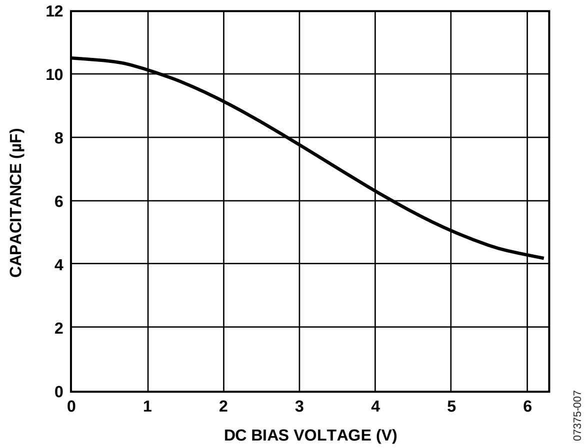


Figure 30. Typical Capacitor Performance

The peak-to-peak output voltage ripple for the selected output capacitor and inductor values is calculated using the following equation:

$$V_{RIPPLE} = \frac{I_{RIPPLE}}{8 \times f_{SW} \times C_{OUT}} \approx \frac{V_{IN}}{(2\pi \times f_{SW})^2 \times L \times C_{OUT}}$$

Capacitors with lower equivalent series resistance (ESR) are preferred to guarantee low output voltage ripple, as shown in the following equation:

$$ESR_{COUT} \leq \frac{V_{RIPPLE}}{I_{RIPPLE}}$$

The effective capacitance needed for stability, which includes temperature and dc bias effects, is 7 µF.

Table 7. Suggested 10 µF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM188R60J106	0603	6.3
Taiyo Yuden	X5R	JMK107BJ106	0603	6.3
TDK	X5R	C1608JB0J106K	0603	6.3

Input Capacitor

Higher value input capacitors help to reduce the input voltage ripple and improve transient response. Maximum input capacitor current is calculated using the following equation:

$$I_{CIN} \geq I_{LOAD(MAX)} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}}$$

To minimize supply noise, place the input capacitor as close to the VIN pin of the ADP2108 as possible. As with the output capacitor, a low ESR capacitor is recommended. The list of recommended capacitors is shown in Table 8.

Table 8. Suggested 4.7 µF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM188R60J475	0603	6.3
Taiyo Yuden	X5R	JMK107BJ475	0603	6.3
TDK	X5R	C1608X5R0J475	0603	6.3

THERMAL CONSIDERATIONS

Because of the high efficiency of the ADP2108, only a small amount of power is dissipated inside the ADP2108 package, which reduces thermal constraints.

However, in applications with maximum loads at high ambient temperature, low supply voltage, and high duty cycle, the heat dissipated in the package is great enough that it may cause the junction temperature of the die to exceed the maximum junction temperature of 125°C. If the junction temperature exceeds 150°C, the converter goes into thermal shutdown. It recovers when the junction temperature falls below 130°C.

The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to power dissipation, as shown in the following equation:

$$T_J = T_A + T_R$$

where:
T_J is the junction temperature.
T_A is the ambient temperature.
T_R is the rise in temperature of the package due to power dissipation.

The rise in temperature of the package is directly proportional to the power dissipation in the package. The proportionality constant for this relationship is the thermal resistance from the junction of the die to the ambient temperature, as shown in the following equation:

$$T_R = \theta_{JA} \times P_D$$

where:
T_R is the rise in temperature of the package.
θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature of the package.
P_D is the power dissipation in the package.

PCB LAYOUT GUIDELINES

Poor layout can affect ADP2108 performance, causing electromagnetic interference (EMI) and electromagnetic compatibility (EMC) problems, ground bounce, and voltage losses. Poor layout can also affect regulation and stability. A good layout is implemented using the following rules:

- Place the inductor, input capacitor, and output capacitor close to the IC using short tracks. These components carry high switching frequencies, and large tracks act as antennas.
- Route the output voltage path away from the inductor and SW node to minimize noise and magnetic interference.
- Maximize the size of ground metal on the component side to help with thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.

EVALUATION BOARD

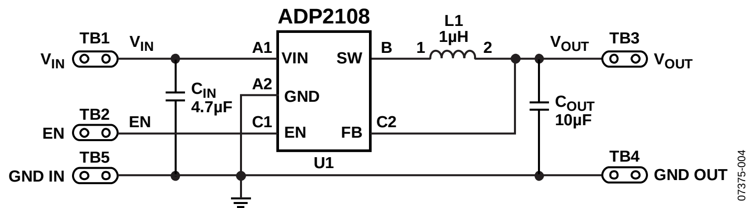


Figure 31. Evaluation Board Schematic

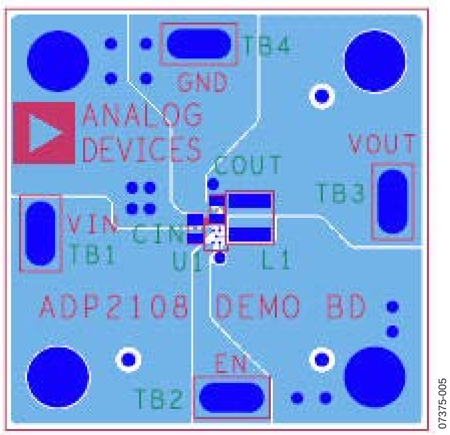


Figure 32. *Recommended* WLCSP Top Layer

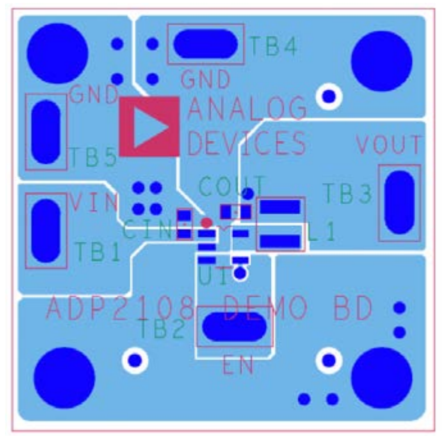


Figure 34. Recommended TSOT Top Layer

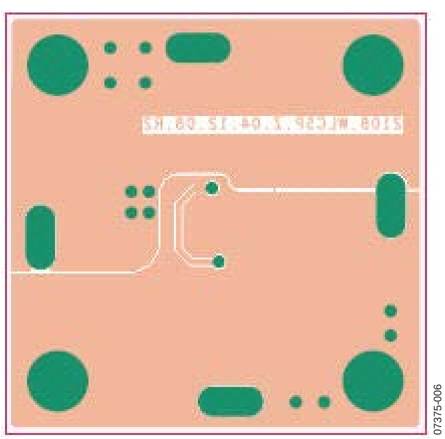


Figure 33. Recommended WLCSP Bottom Layer

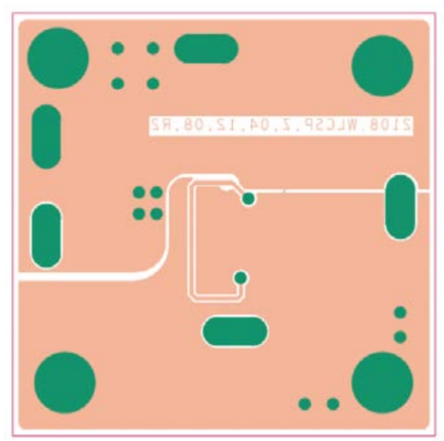


Figure 35. Recommended TSOT Bottom Layer

OUTLINE DIMENSIONS

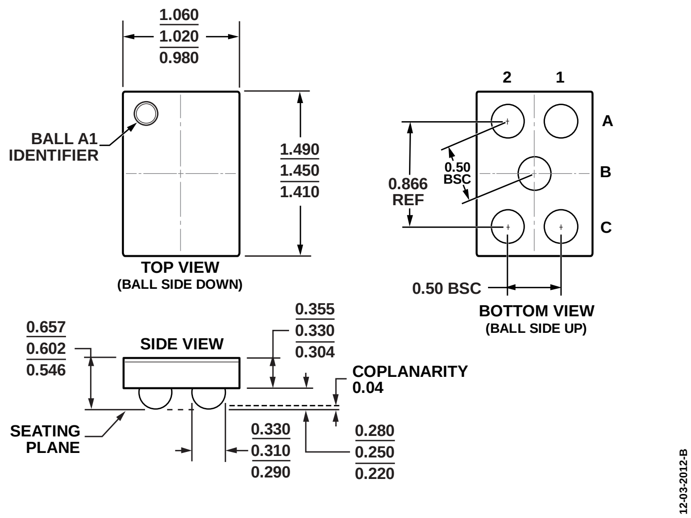


Figure 36. 5-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-5-3)
Dimensions shown in millimeters

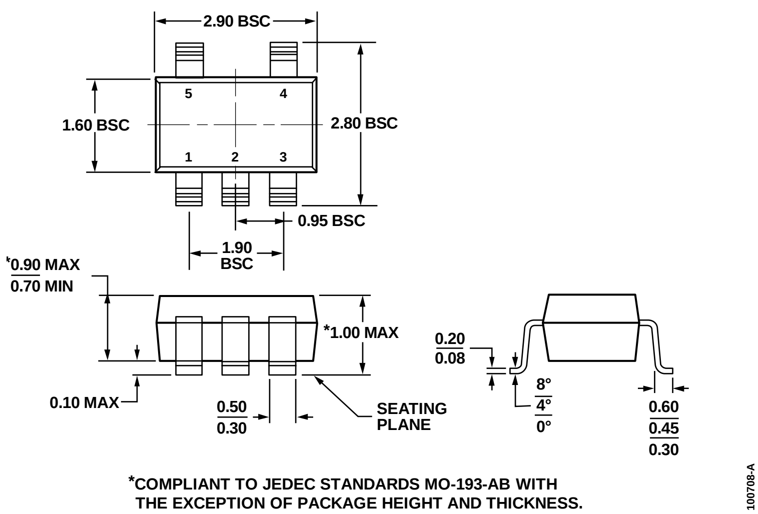


Figure 37. 5-Lead Thin Small Outline Transistor Package [TSOT]
(UJ-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage (V)	Package Description	Package Option	Branding
ADP2108ACBZ-1.0-R7	−40°C to +125°C	1.0	5-Ball Wafer Level Chip Scale Package [WLCSP]	CB-5-3	LA6
ADP2108ACBZ-1.1-R7	−40°C to +125°C	1.1	5-Ball Wafer Level Chip Scale Package [WLCSP]	CB-5-3	LA7
ADP2108ACBZ-1.2-R7	−40°C to +125°C	1.2	5-Ball Wafer Level Chip Scale Package [WLCSP]	CB-5-3	LA8
ADP2108ACBZ-1.3-R7	−40°C to +125°C	1.3	5-Ball Wafer Level Chip Scale Package [WLCSP]	CB-5-3	LA9
ADP2108ACBZ-1.5-R7	−40°C to +125°C	1.5	5-Ball Wafer Level Chip Scale Package [WLCSP]	CB-5-3	LAA
ADP2108ACBZ-1.8-R7	−40°C to +125°C	1.8	5-Ball Wafer Level Chip Scale Package [WLCSP]	CB-5-3	LAD
ADP2108ACBZ-1.82-R7	−40°C to +125°C	1.82	5-Ball Wafer Level Chip Scale Package [WLCSP]	CB-5-3	LAE
ADP2108ACBZ-2.3-R7	−40°C to +125°C	2.3	5-Ball Wafer Level Chip Scale Package [WLCSP]	CB-5-3	LAF
ADP2108ACBZ-2.5-R7	−40°C to +125°C	2.5	5-Ball Wafer Level Chip Scale Package [WLCSP]	CB-5-3	LAG
ADP2108ACBZ-3.0-R7	−40°C to +125°C	3.0	5-Ball Wafer Level Chip Scale Package [WLCSP]	CB-5-3	LD9
ADP2108ACBZ-3.3-R7	−40°C to +125°C	3.3	5-Ball Wafer Level Chip Scale Package [WLCSP]	CB-5-3	LAH
ADP2108AUJZ-1.0-R7	−40°C to +125°C	1.0	5-Lead Small Outline Package [TSOT]	UJ-5	LA6
ADP2108AUJZ-1.1-R7	−40°C to +125°C	1.1	5-Lead Small Outline Package [TSOT]	UJ-5	LA7
ADP2108AUJZ-1.2-R7	−40°C to +125°C	1.2	5-Lead Small Outline Package [TSOT]	UJ-5	LA8
ADP2108AUJZ-1.3-R7	−40°C to +125°C	1.3	5-Lead Small Outline Package [TSOT]	UJ-5	LA9
ADP2108AUJZ-1.5-R7	−40°C to +125°C	1.5	5-Lead Small Outline Package [TSOT]	UJ-5	LAA
ADP2108AUJZ-1.8-R7	−40°C to +125°C	1.8	5-Lead Small Outline Package [TSOT]	UJ-5	LAD
ADP2108AUJZ-1.82-R7	−40°C to +125°C	1.82	5-Lead Small Outline Package [TSOT]	UJ-5	LAE
ADP2108AUJZ-2.3-R7	−40°C to +125°C	2.3	5-Lead Small Outline Package [TSOT]	UJ-5	LAF
ADP2108AUJZ-2.5-R7	−40°C to +125°C	2.5	5-Lead Small Outline Package [TSOT]	UJ-5	LAG
ADP2108AUJZ-3.0-R7	−40°C to +125°C	3.0	5-Lead Small Outline Package [TSOT]	UJ-5	LD9
ADP2108AUJZ-3.3-R7	−40°C to +125°C	3.3	5-Lead Small Outline Package [TSOT]	UJ-5	LAH
ADP2108-1.0-EVALZ		1.0	Evaluation Board for 1.0 V [WLCSP]		
ADP2108-1.1-EVALZ		1.1	Evaluation Board for 1.1 V [WLCSP]		
ADP2108-1.2-EVALZ		1.2	Evaluation Board for 1.2 V [WLCSP]		
ADP2108-1.3-EVALZ		1.3	Evaluation Board for 1.3 V [WLCSP]		
ADP2108-1.5-EVALZ		1.5	Evaluation Board for 1.5 V [WLCSP]		
ADP2108-1.8-EVALZ		1.8	Evaluation Board for 1.8 V [WLCSP]		
ADP2108-1.82-EVALZ		1.82	Evaluation Board for 1.82 V [WLCSP]		
ADP2108-2.3-EVALZ		2.3	Evaluation Board for 2.3 V [WLCSP]		
ADP2108-2.5-EVALZ		2.5	Evaluation Board for 2.5 V [WLCSP]		
ADP2108-3.0-EVALZ		3.0	Evaluation Board for 3.0 V [WLCSP]		
ADP2108-3.3-EVALZ		3.3	Evaluation Board for 3.3 V [WLCSP]		
ADP2108UJZ-REDYKIT			Evaluation Board for Fixed Output Voltage, 1.2 V and 3.3 V [TSOT]		

[1] Z = RoHS Compliant Part.

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